ART2932

User's Manual

Beijing ART Technology Development Co., Ltd.

Contents

Chapter 1 Overview

In the fields of Real-time Signal Processing, Digital Image Processing and others, high-speed and high-precision data acquisition modules are demanded. ART2932 data acquisition module, which brings in advantages of similar products that produced in China and other countries, is convenient for use, high cost and stable performance.

ART2932 is a data acquisition module based on PC104 bus. It can be directly connected with PC104 interface of computer to constitute the laboratory, product quality testing center and systems for different areas of data acquisition, waveform analysis and processing. It may also constitute the monitoring system for industrial production process.

Unpacking Checklist

Check the shipping carton for any damage. If the shipping carton and contents are damaged, notify the local dealer or sales for a replacement. Retain the shipping carton and packing material for inspection by the dealer.
Check for the following items in the package. If there are any missing items, contact your local dealer or sales.

- ART2932 Data Acquisition Board
- ART Disk
  a) user's manual (pdf)
  b) drive
  c) catalog
- Warranty Card

FEATURES

Analog Input

- Converter Type: AD7321
- Input Range: ±10V, ±5V (default), ±2.5, 0~10V
- 12-bit resolution
- Sampling Rate: 1Hz~250KHz
  Note: each channel actual sampling rate = sampling rate/the number of sampling channels
- Analog Input Mode: 16SE/8DI
- Data Read Mode: non-empty, half-full inquiry mode
- Memory Depth: 8K word FIFO memory
- Memory Signs: full, non-empty and half-full
- AD Mode: continuum sampling , grouping sampling
- Group Interval: software-configurable, minimum value is sampling period, maximum value is 3276us
- Loops of Group: software-configurable, minimum value is one time , maximum value is 255 times
- Trigger Mode: software trigger, hardware trigger (external trigger)
- Trigger Type: level trigger , edge trigger
- Trigger Direction: negative, positive, positive and negative trigger
- Trigger Source: ATR, DTR
- Analog Trigger Source (ATR)Input Range: <AO0 and >AO1 (AO1>AO0)
- Trigger Source DTR Input Range: standard TTL level
- AD Conversion Time: ≤1.6μs
- Amplifier Set-up Time: 785ns (0.001%) (max)

- Programmable Gain: 1, 2, 4, 8 (AD8251 default) or 1, 2, 5, 10 (AD8250) or 1, 10, 100, 1000 (AD8253)
- Analog Input Impedance: 10MΩ
- Non-linear error: ±1LSB(Max)
- System Measurement Accuracy: 0.01%
- Operating Temperature Range: 0℃~55℃
- Storage Temperature Range: -20℃~70℃

Analog Output

- Converter Type: AD5724
- Output Range: ±10.8V, ±10V, ±5V, 0~10.8V , 0~10V, 0~5V
- 12-bit resolution
- Channel No.: 4-channel
- Non-linear error: ±1LSB(Maximum)
- Output Error (full-scale): ±1LSB
- Operating Temperature Range: 0℃~55℃
- Storage Temperature Range: -20℃~70℃

Digital Input

- Channel No.: 8-ch
- Electric Standard: TTL compatible
- High Voltage: ≧2V
- Low Voltage: ≦0.8V

Digital Output

- Channel No.: 8-ch
- Electrical Standard: TTL compatible
- High Voltage: ≧3.8V
- Low Voltage: ≦0.44V
- Power-on Reset

CNT Counter/timer

- 16-bit counter/timer, 3 independent subtraction counters
- Count Mode: 6 modes
- Electrical Standard: TTL level
- Input Electrical Standards: low level ≦0.8V, high level ≧2V
- Output Electrical Standards: low level ≦0.5V, high level ≧2.4V
- Clock Source: frequency range 1Hz~10MHz
- Gate: rising edge, high level, low level
- Counter Output: high level, low level

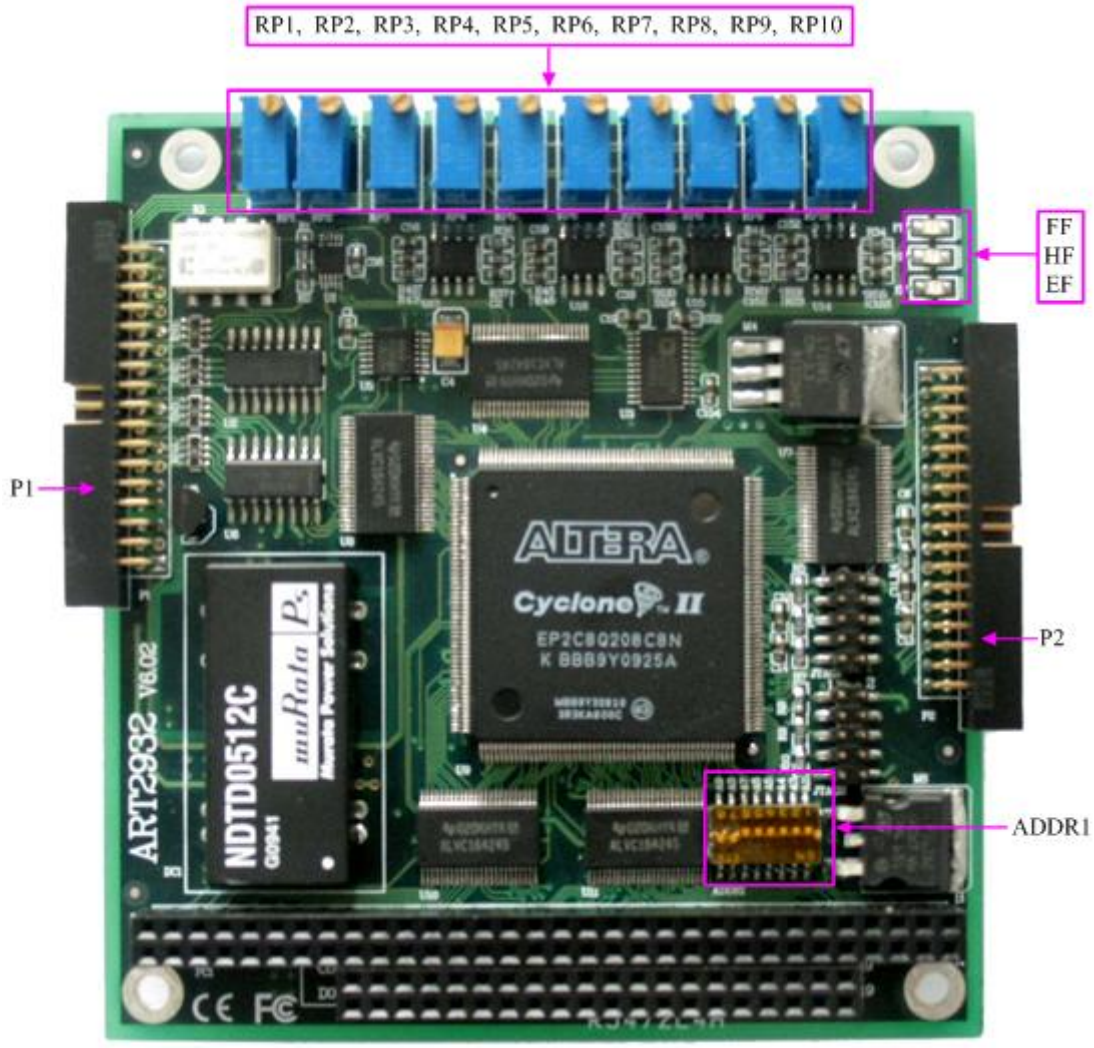
Other Features

Board Clock Oscillation: 40MHz

Dimension: 90.3mm (L)*96mm (W) *16mm (H)

Chapter 2 Components Layout Diagram and a Brief Description

2.1 The Main Component Layout Diagram



2.2 The Function Description for the Main Component

2.2.1 Signal Input and Output Connectors

P1: analog signal input/output connectors
P2: digital input/output port

2.2.2 Potentiometer

RP1: AD analog signal input zero-point adjustment potentiometer
RP2: AD analog signal input full-scale adjustment potentiometer
RP3: AO0 analog signal output zero-point adjustment potentiometer
RP4: AO0 analog signal output full-scale adjustment potentiometer
RP5: AO1 analog signal output zero-point adjustment potentiometer
RP6: AO1 analog signal output full-scale adjustment potentiometer
RP7: AO2 analog signal output zero-point adjustment potentiometer
RP8: AO2 analog signal output full-scale adjustment potentiometer
RP7: AO3 analog signal output zero-point adjustment potentiometer
RP8: AO3 analog signal output full-scale adjustment potentiometer

2.2.3 Board Base Address Selection

ADDR1: board base address DIP switches. Board base address can be set to binary code which from 200H to 3E0H be divided by 16, board base address defaults 300H, will occupy the base address of the date of 28 consecutive I/O addresses. Switch No. 5, 6, 7, 8 correspond to address bits A6, A7, A8, A9, are the base address of selector switch, Switch No. 1, 2, 3, 4 correspond to address bits A2, A3, A4, A5, are reserved bit.

Board base address selection is as follows: when the ADDR1 switches dial to "ON" that means high virtual value is 1, the switch to the other side means the low virtual is 0.

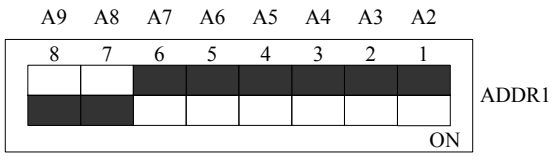
Board base address selection switch ADDR1shown as following:

Base address configuration methods

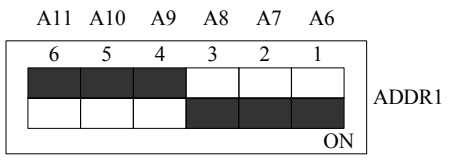
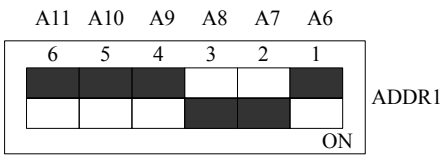
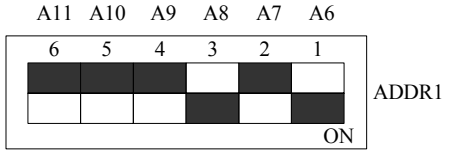
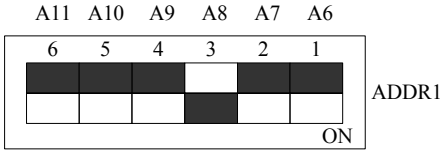
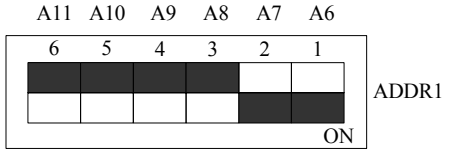
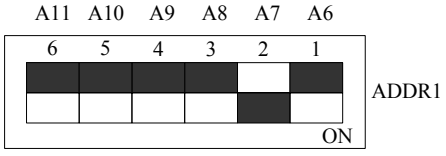
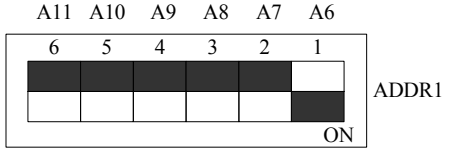
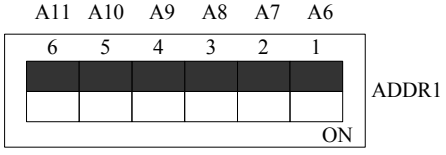
Address bit	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
X is configurable bit	unused	unused	x	x	x	x	0	0	0	0	0	0
	The third hex bits				The second hex bits				The first hex bits			

Note: in the table, the bit which is labeled "0"is a fixed value, only the bit that labeled "x" can be changed by the ADDR1

For example, the default base addresses is300H, A8, A9= "ON", shown as the following:



Common base address

Adr	ADDR1	Adr	ADDR1
200H		240H	
280H		2C0H	
300H		340H	
380H		3C0H	

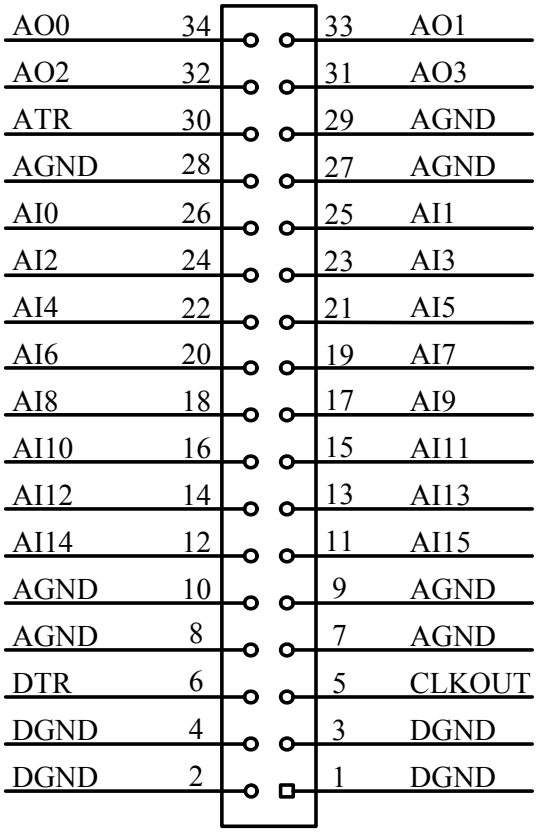
2.2.4 Status Lights

EF: FIFO non-empty indicator
HF: FIFO half-full indicator
FF: FIFO overflow indicator

Chapter 3 Signal Connectors

3.1 The Definition of Signal Input and Output Connectors

34-pin P1 definition

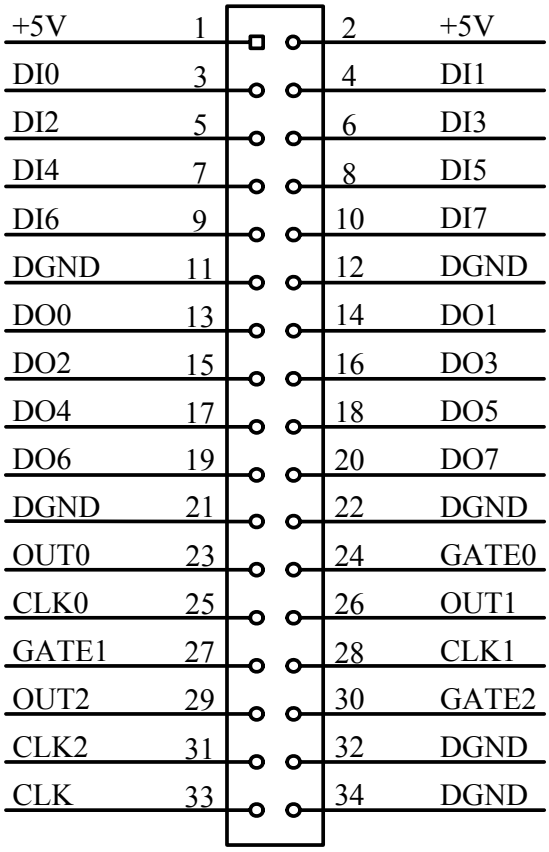


Pin definition:

Pin name	Type	Pin function definition
AI0～AI15	Input	AD analog input, reference ground is AGND.
AO0～AO3	Output	DA analog output.
AGND		Analog ground. This AGND pin should be connected to the system's AGND plane.
DGND		Digital ground. Ground reference for Digital circuitry. This DGND pin should be connected to the system's DGND plane.
CLK_OUT	Output	Internal clock output, when allow clock output, it is internal clock output, otherwise it is CNT counter output. DGND for reference ground.
ATR	Input	Analog trigger signal input, choose AGND as reference ground.
DTR	Input	Digital trigger signal input, choose DGND as reference ground.

3.2 Digital Input/Output Connectors

34-pin P2 definition



Pin definition about P1:

Pin Name	Pin Feature	Pin Function Definition
DI0～DI7	Input	Digital input.
DO0～DO7	Input	Digital output.
DGND	GND	Digital ground.
CLK0～CLK2	Input	Counter 0~3 channels clock input.
GATE0～GATE2	Input	Counter 0~3 channels gate.
OUT0～OUT2	Output	Counter 0~3 channels output.
+5V	Output	Output +5V.

Chapter 4 Connection Ways for Each Signal

4.1 AD Single-ended Input Connection

Single-ended mode can achieve a signal input by one channel, and several signals use the common reference ground. This mode is widely applied in occasions of the small interference and relatively many channels.

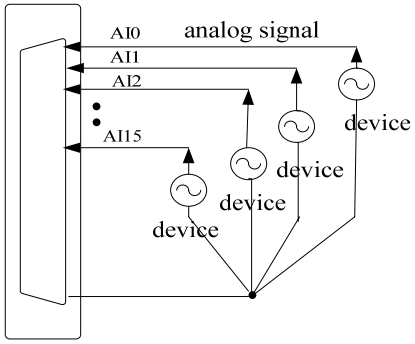


Figure 4.1 single-ended input connection

4.2 AD Double-ended Input Mode

Double-ended input mode, which was also called differential input mode, uses positive and negative channels to input a signal. This mode is mostly used when biggish interference happens and the channel numbers are few. Single-ended/double-ended mode can be set by the software, please refer to ART2932 software manual.

According to the diagram below, ART2932 board can be connected as analog voltage double-ended input mode, which can effectively suppress common-mode interference signal to improve the accuracy of acquisition. Positive side of the 8-channel analog input signal is connected to AI0~AI7, the negative side of the analog input signal is connected to AI8~AI15, equipments in industrial sites share the AGND with ART2932 board.

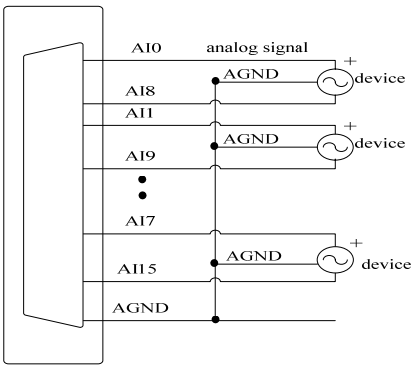


Figure 4.2 double-ended input connection

4.3 Other Connections

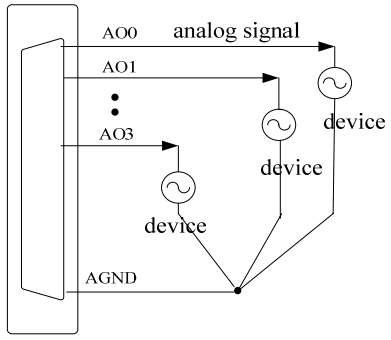


Figure 4.3 analog signal output connection

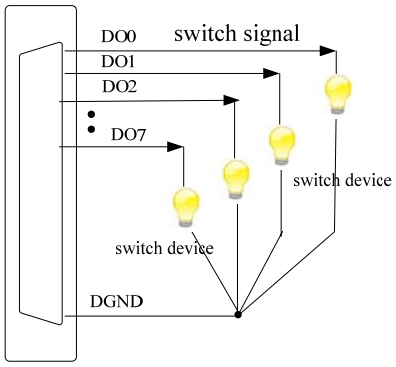


Figure 4.5 digital signal output connection

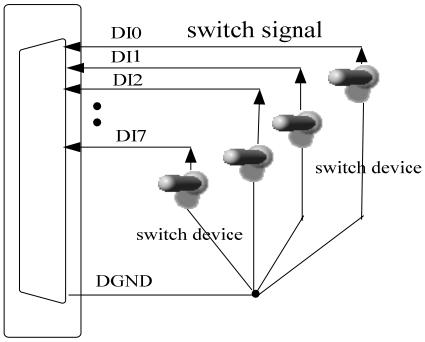


Figure 4.4 digital signal input connection

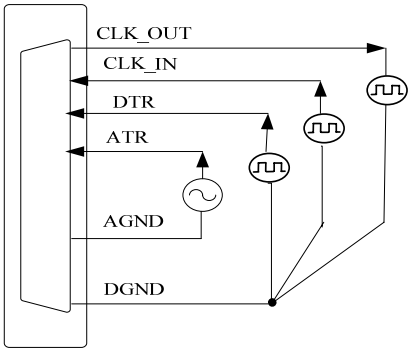


Figure 4.6 Clock Input/Output and Trigger Signal Connection

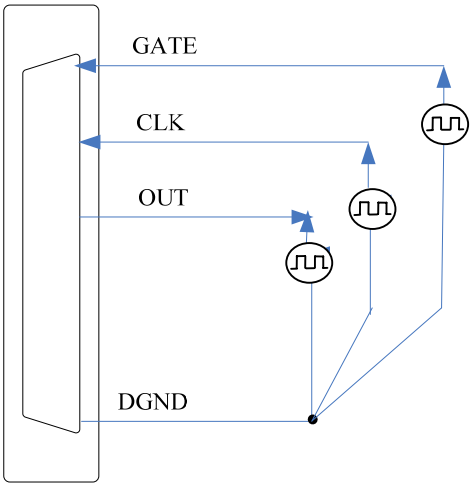
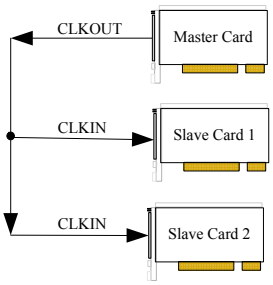


Figure 4.7 CNT Timer/Counter signal connection

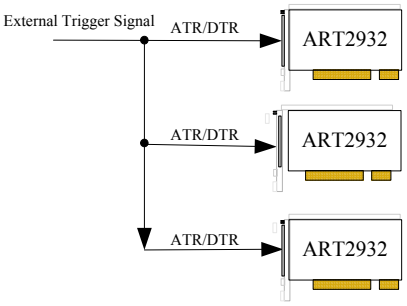
4.4 Methods of Realizing the Multi-card Synchronization

Three methods can realize the synchronization for the ART2932, the first method is using the cascade master-slave card, the second one is using the common external trigger, and the last one is using the common external clock. When using master-slave cascade card programs, the master card generally uses the internal clock source model, while the slave card uses the external clock source mode. After the master card and the slave card are initialized according to the

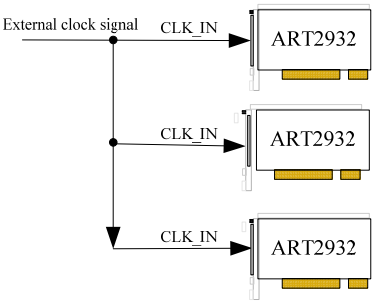
corresponding clock source mode. At first, start all the slave cards, as the main card has not been activated and there is no output clock signal, so the slave card enters the wait state until the main card was activated. At this moment, the multi-card synchronization has been realized. When you need to sample more than channels of a card, you could consider using the multi-card cascaded model to expand the number of channels.



When using the common external trigger, please make sure all parameters of different ART2932 are the same. At first, configure hardware parameters, and use analog or digital signal triggering (ATR or DTR), then connect the signal that will be sampled by ART2932, input triggering signal from ART pin or DTR pin, then click “Start Sampling” button, at this time, ART2932 does not sample any signal but waits for external trigger signal. When each module is waiting for external trigger signal, use the common external trigger signal to startup modules, at last, we can realize synchronization data acquisition in this way. See the following figure:



When using the common external clock trigger, please make sure all parameters of different ART2932 are the same. At first, configure hardware parameters, and use external clock, then connect the signal that will be sampled by ART2932, input trigger signal from ART pin or DTR pin, then click “Start Sampling” button, at this time, ART2932 does not sample any signal, but wait for external clock signal. When each module is waiting for external clock signal, use the common external clock signal to startup modules, at last, we realize synchronization data acquisition in this way. See the following figure:



Chapter 5 The Instruction of the AD Trigger Function

5.1 AD Internal Trigger Mode

When AD is in the initialization, if the AD hardware parameter ADPara.TriggerMode = ART2932_TRIGMODE_SOFT, we can achieve the internal trigger acquisition. In this function, when calling the StartDeviceProAD function, it will generate AD start pulse, AD immediately access to the conversion process and not wait for the conditions of any other external hardware. It also can be interpreted as the software trigger.

As for the specific process, please see the figure below, the cycle of the AD work pulse is decided by the sampling frequency.

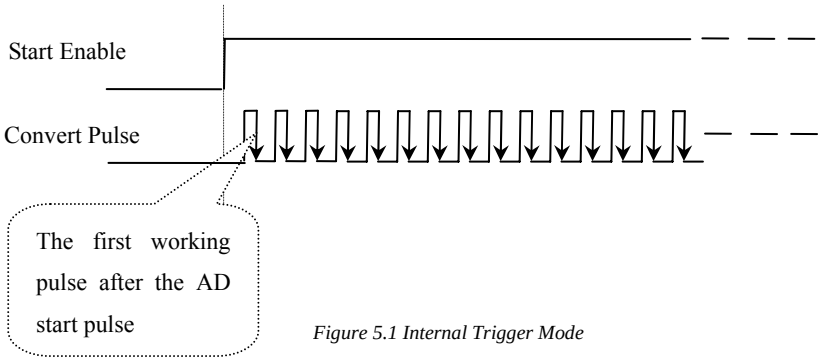


Figure 5.1 Internal Trigger Mode

5.2 AD External Trigger Mode

When AD is in the initialization, if the AD hardware parameter ADPara.TriggerMode = ART2932_TRIGMODE_POST, we can achieve the external trigger acquisition. In this function, when calling the StartDeviceProAD function, AD will not immediately access to the conversion process but wait for the external trigger source signals accord with the condition, then start converting the data. It also can be interpreted as the hardware trigger. Trigger source includes the DTR (Digital Trigger Source) and ATR (Analog Trigger Source).

5.2.1 ATR Trigger

When the trigger signal is the analog signal, using the ATR trigger source. Trigger level needs to be set when using the ATR trigger source, two channels' output voltages of DA (AO0 and AO1) codetermines the trigger level; in this case, we need set 0-channel output voltage higher than 1-channel output voltage. There are two trigger types: edge trigger and level trigger

Edge Trigger Function

Edge trigger is to capture the characteristics of the changes between the trigger source signal and the trigger level signal to trigger AD conversion.

When ADPara.TriggerDir = ART2932_TRIGDIR_NEGATIVE, choose the trigger mode as the falling edge trigger. That is, when the ATR trigger signal is from higher than 0-channel output voltage to lower than 1-channel output voltage, AD will immediately access to the conversion process, and its follow-up changes have no effect on AD acquisition.

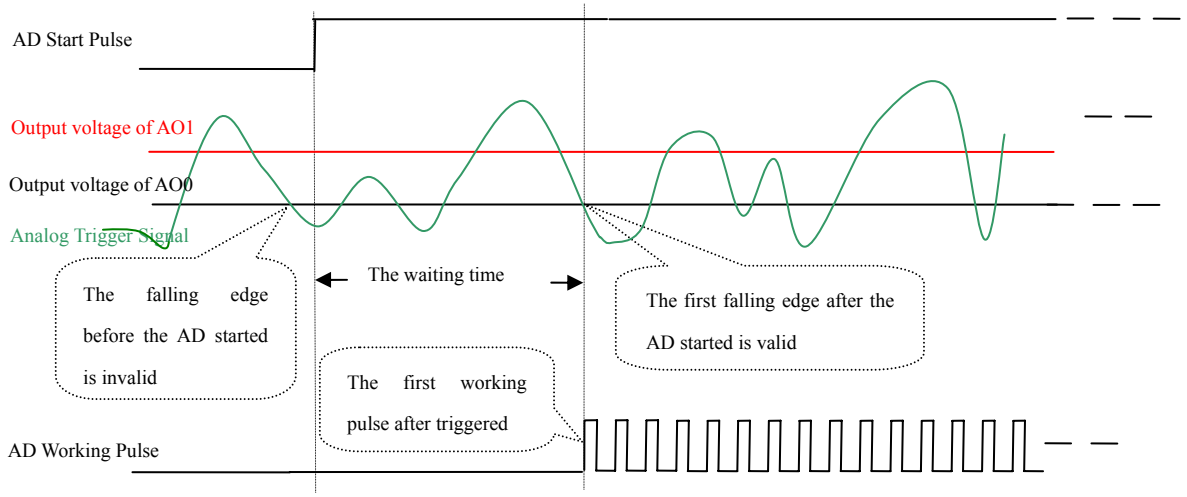


Figure 5.2.1 Falling edge Trigger

When ADPara.TriggerDir = ART2932_TRIGDIR_POSITIVE, choose the trigger mode as rising edge trigger. That is, when the ATR trigger signal is from lower than 0-channel output voltage to higher than 1-channel output voltage, AD will immediately access to the conversion process, and its follow-up changes have no effect on AD acquisition.

When ADPara.TriggerDir = ART2932_TRIGDIR_POSIT_NEGAT, choose the trigger mode as rising or falling edge trigger. That is, when the ATR trigger signal is from higher than 1-channel output voltage to lower than 0-channel output voltage, or when the ATR trigger signal is from lower than 0-channel output voltage to higher than 1-channel output voltage, AD will immediately access to the conversion process, and its follow-up changes have no effect on AD acquisition. This function can be used in the case that the acquisition will occur if the exoteric signal changes.

Triggering Level Function

Level trigger is to capture the condition that trigger signal is higher or lower than the trigger level to trigger AD conversion.

When ADPara.TriggerDir = ART2932_TRIGDIR_NEGATIVE, it means the trigger level is low. When ATR trigger signal is smaller than 0-channel output voltage, AD is in the conversion process, once the trigger signal is higher than 1-channel output voltage, AD conversion will automatically stop, when the trigger signal is smaller than 0-channel output voltage again, AD will re-access to the conversion process, that is, only converting the data when the trigger signal is smaller than 0-channel output voltage.

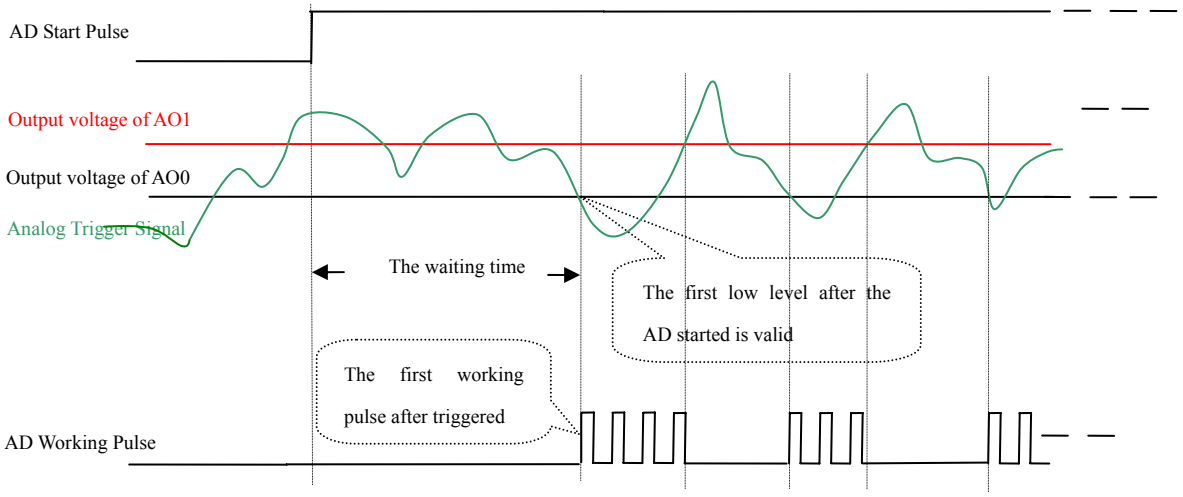


Figure 5.2.2 Low Level Trigger

When ADPara.TriggerDir = ART2932_TRIGDIR_POSITIVE, it means the trigger level is high. When ATR trigger signal is higher than 1-channel output voltage, AD is in the conversion process, once the trigger signal is smaller than 0-channel output voltage, AD conversion will automatically stop, when the trigger signal is higher than 1-channel output voltage again, AD will re-access to the conversion process, that is, only converting the data when the trigger signal is higher than 1-channel output voltage.

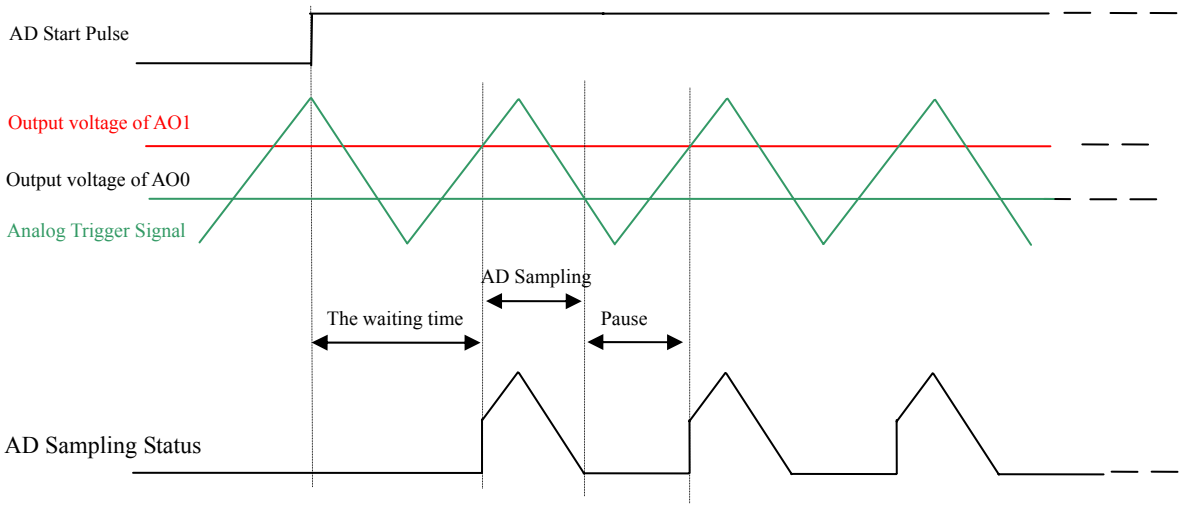


Figure 5.2.3 High Level Trigger

When ADPara.TriggerDir = ART2932_TRIGDIR_POSIT_NEGAT, it means the trigger level is low or high. The effect is the same as the internal software trigger.

5.2.2 DTR Trigger

When the trigger signal is the digital signal (standard TTL-level), using the DTR trigger source.

Edge Trigger Function

Edge trigger is to capture the characteristics of the changes between the trigger source signal and the trigger level signal to trigger AD conversion.

When ADPara.TriggerDir = ART2932_TRIGDIR_NEGATIVE, choose the trigger mode as the falling edge trigger. That is, when the DTR trigger signal is on the falling edge, AD will immediately access to the conversion process, and its follow-up changes have no effect on AD acquisition.

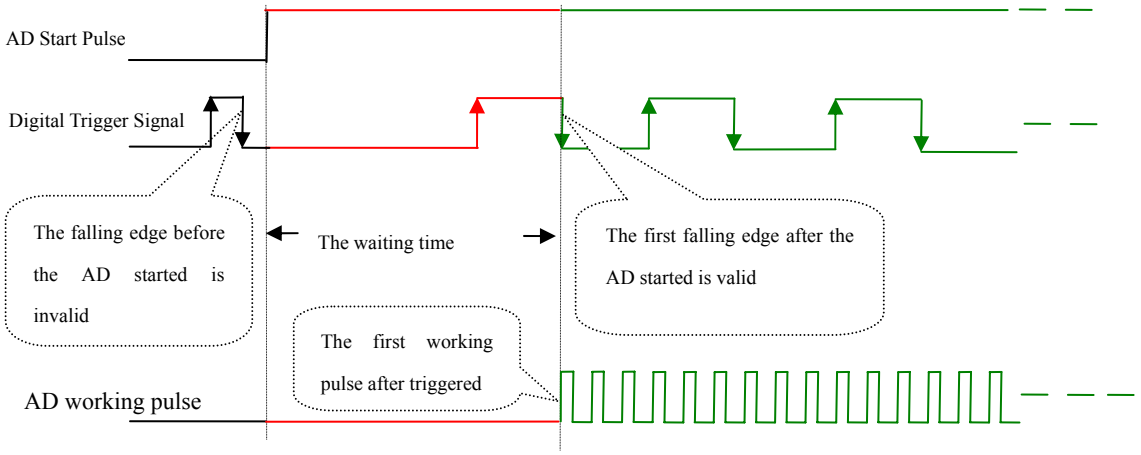


Figure 5.2.4 Falling edge Trigger

When ADPara.TriggerDir = ART2932_TRIGDIR_POSITIVE, choose the trigger mode as rising edge trigger. That is, when the DTR trigger signal is on the rising edge, AD will immediately access to the conversion process, and its follow-up changes have no effect on AD acquisition.

When ADPara.TriggerDir = ART2932_TRIGDIR_POSIT_NEGAT, choose the trigger mode as rising or falling edge trigger. That is, when the DTR trigger signal is on the rising or falling edge, AD will immediately access to the conversion process, and its follow-up changes have no effect on AD acquisition. This function can be used in the case that the acquisition will occur if the exoteric signal changes.

Triggering Level Function

Level trigger is to capture the condition that trigger signal is higher or lower than the trigger level to trigger AD conversion.

When ADPara.TriggerDir = ART2932_TRIGDIR_NEGATIVE, it means the trigger level is low. When DTR trigger signal is in low level, AD is in the conversion process, once the trigger signal is in the high level, AD conversion will automatically stop, when the trigger signal is in the low level again, AD will re-access to the conversion process, that is, only converting the data when the trigger signal is in the low level.

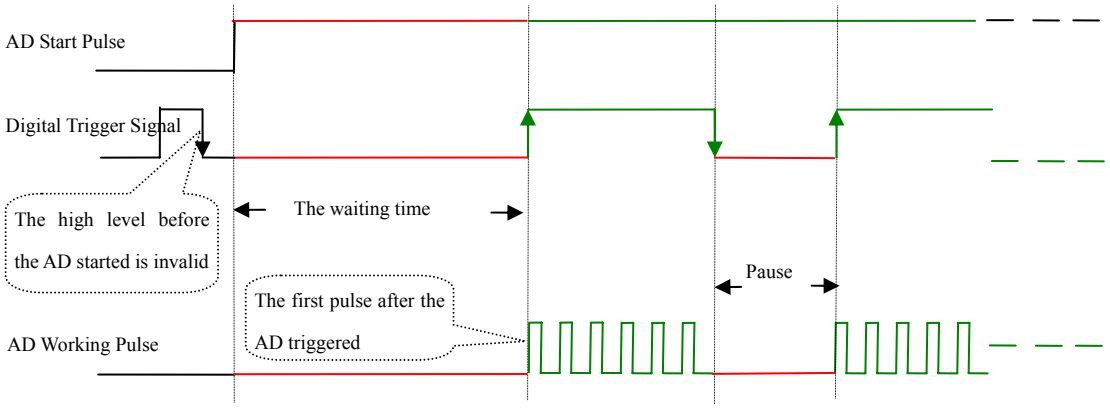


Figure 5.2.4 High Level Trigger

When ADPara.TriggerDir = ART2932_TRIGDIR_POSITIVE, it means the trigger level is high. When DTR trigger signal is in high level, AD is in the conversion process, once the trigger signal is in the low level, AD conversion will automatically stop, when the trigger signal is in the high level again, AD will re-access to the conversion process, that is, only converting the data when the trigger signal is in the high level.

When ADPara.TriggerDir = ART2932_TRIGDIR_POSIT_NEGAT, it means the trigger level is low or high. The effect is the same as the internal software trigger.

Chapter 6 Methods of using AD Internal and External Clock Function

6.1 Internal Clock Function of AD

Internal Clock Function refers to the use of on-board clock oscillator and the clock signals which are produced by the user-specified frequency to trigger the AD conversion regularly. To use the clock function, the hardware parameters ADPara.ClockSource = ART2932 _CLOCKSRC_IN should be installed in the software. The frequency of the clock in the software depends on the hardware parameters ADPara.Frequency. For example, if Frequency = 100000, that means AD work frequency is 100000Hz (that is, 100 KHz, 10 us/point).

6.2 External Clock Function of AD

External Clock Function refers to the use of the outside clock signals to trigger the AD conversion regularly. The clock signals are provide by the CLKIN pin of the CN1 connector. The outside clock can be provided by ART2932 clock output (CLKOUT of P1), as well as other equipments, for example clock frequency generators. To use the external clock function, the hardware parameters ADPara.ClockSource = ART2932_CLOCKSRC_OUT should be installed in the software. The clock frequency depends on the frequency of the external clock, and the clock frequency on-board (that is, the frequency depends on the hardware parameters ADPara.Frequency) only functions in the packet acquisition mode and its sampling frequency of the AD is fully controlled by the external clock frequency.

6.3 Methods of Using AD Continuum and Grouping Sampling Function

6.3.1 AD Continuum Sampling Function

The continuous acquisition function means the sampling periods for every two data points are completely equal in the sampling process of AD, that is, completely uniform speed acquisition, without any pause, so we call that continuous acquisition.

To use the continuous acquisition function, the hardware parameters ADPara.ADMode = ART2932_ADMODE_SEQUENCE should be installed in the software. For example, in the internal clock mode, hardware parameters ADPara.Frequency = 100000 (100KHz) should be installed, and 10 microseconds after the AD converts the first data point, the second data point conversion starts, and then 10 microseconds later the third data point begins to convert, and so on.

The formula for calculating the external signal frequency is as follows:

Under the internal clock mode:

External signal frequency = AD sampling frequency / (cycle signal points * the total number of channels)

External signal cycle= 1/ external signal frequency

Under the external clock mode:

External signal frequency = AD sampling frequency / (cycle signal points * the total number of channels)

External signal cycle= 1/ external signal frequency

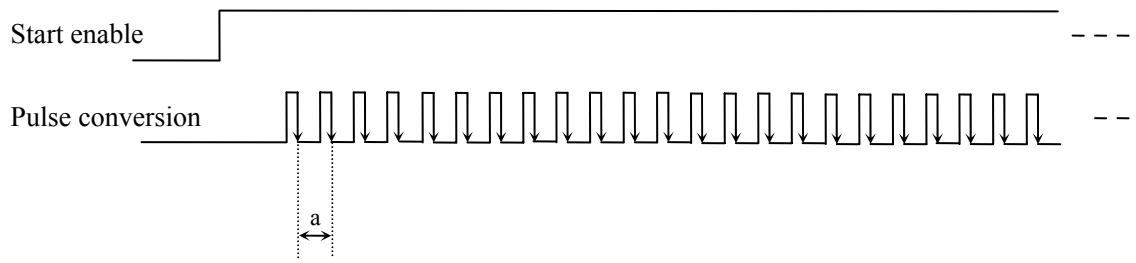


Figure 6.1continuous acquisition in internal clock

Note: a-- sample cycle

6.3.2 AD Grouping Sampling Function

Grouping acquisition (pseudo-synchronous acquisition) function refers to the sampling clock frequency conversion among the channels of the group in the AD sampling process, and also a certain waiting time exists between every two groups, this period of time is known as the Inter-group Spacing. Cycles of Group refers to numbers of the cycle acquisition for each channel in the same group. In the internal clock mode and the fixed-frequency external clock mode, the time between the groups is known as group cycles. The conversion process of this acquisition mode as follows: a short time stop after the channels conversion in the group (that is, Inter-group Group Interval), and then converting the next group, followed by repeated operations in order, so we call it grouping acquisition.

The purpose of the application of the grouping acquisition is that: at a relatively slow frequency, to ensure that all of the time difference between channels to become smaller in order to make the phase difference become smaller, thus to ensure the synchronization of the channels, so we also say it is the pseudo-synchronous acquisition function. In a group, the higher the sampling frequency is, the longer inter-group interval is, and the better the relative synchronization signal is. The sampling frequency in a group depends on ADPara. Frequency, the cycles of a group depends on ADPara. Loops of Group and the inter-group interval depend on ADPara. Group Interval.

Based on the grouping function, it can be divided into the internal clock mode and the external clock mode. Under the internal clock mode, the group cycle is decided by the internal clock sampling period, the total number of sampling channels, group cycles and inter-group interval together. In each cycle of a group, AD only collects a set of data. Under the external clock mode, external clock cycle ≥ internal clock sampling cycle × the total number of sampling channels × cycles of Group + AD chip conversion time, AD data acquisition is controlled and triggered by external clock. The external clock mode is divided into fixed frequency external clock mode and unfixed frequency external clock mode. Under the fixed frequency external clock mode, the group cycle is the sampling period of the external clock.

The formula for calculating the external signal frequency is as follows:

Under the internal clock mode:
Group Cycle = the internal clock sampling period × the total number of sample channels × group cycles + AD chips conversion time + inter-group interval
External signal cycle = (cycle signal points / group cycles) × Group cycle
External signal frequency = 1 / external signal cycle

Under the external clock mode: (a fixed-frequency external clock)
Group Cycle = external clock cycle
External signal cycle = (cycle signal points / group cycles) × group cycle
External signal frequency = 1 / external signal cycle

Formula Notes:
The internal sampling clock cycle = 1 / (AD Para. Frequency)
The total number of sampling channels = AD Para. Last Channel – AD Para. First Channel + 1
Cycles of Group = AD Para. Loops of Group
AD Chips conversion time = see "AD Analog Input Function" parameter
Inter-group interval = AD Para. Group Interval
Signal Cycle Points = with the display of the waveform signal in test procedures, we can use the mouse to measure the signal cycle points.

Under the internal clock mode, for example, sample two-channel 0, 1, and then 0 and 1 become a group. Sampling frequency (Frequency) = 100000Hz (cycle is 10uS), cycles of group is 1, inter-group interval (Group Interval) = 50uS, then the acquisition process is to collect a set of data first, including a data of channel 0 and a data of channel 1. We need 10uS to sample the two data, 20uS to convert the data from the two channels. After the conversion time of an AD chip, AD will automatically cut-off to enter into the waiting state until the 50uS group interval ends. We start the next group, begin to convert the data of channel 0 and 1, and then enter into the waiting state again, and the conversion is going on in this way, as the diagram following shows:

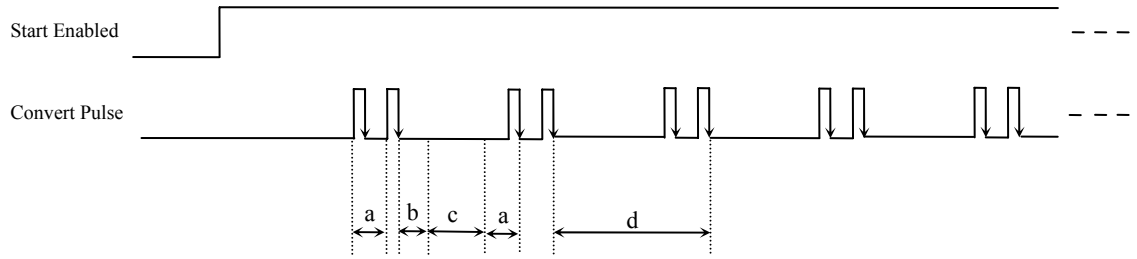


Figure 6.1 Grouping Sampling which grouping cycle No is 1 under the Internal Clock Mode

Note: a— internal clock sample cycle
b— AD chips conversion time
c— inter-group interval
d— group cycle

Change the group cycles into 2, then the acquisition process is to collect the first set of data, including two data of channel 0 and two data of channel 1, the conversion order is 0,1,0,1. We need 10uS to sample each of the four data. After the conversion time of an AD chip, AD will automatically stop to enter into the waiting state until the 50uS group interval ends. We start the next group, begin to convert the data of channel 0 and 1, and then enter into the waiting state again, and the conversion is going on in this way, as the diagram following shows:

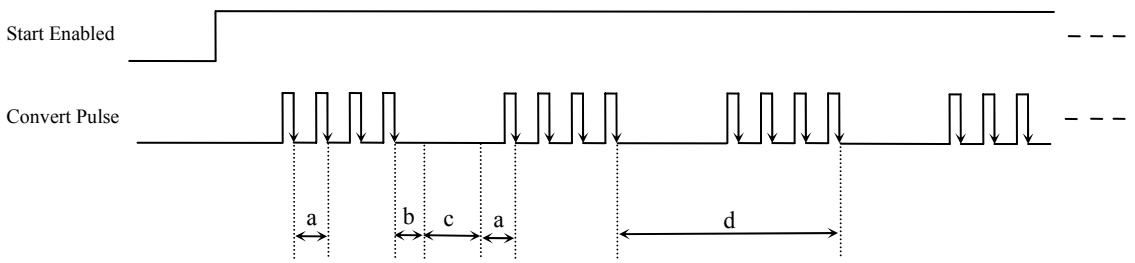


Figure 6.2 Grouping Sampling which grouping cycle No is 2 under the Internal Clock Mode

Notes: a— internal clock sample cycle
b— AD chips conversion time
c— inter-group interval
d— group cycle

Under the external clock mode, the requirement is: the external clock cycle ≥ the internal clock sampling period × the total number of sampling channels× cycles of group + AD chip conversion time, otherwise, the external clock appearing in the group conversion time will be ignored.

Under the fixed-frequency external clock mode, for example, when sampling data of two-channel 0, 1, then channel 0 and channel 1 consist of a group. Sampling frequency (Frequency) = 100000Hz (the cycle is 10uS), cycles of group is 2, then the acquisition process is to collect the first set of data, including two data of channel 0 and two data of channel 1, the order of conversion 0,1,0,1, We need 10uS to sample the four data and 40uS to convert of the four data. After the conversion time of an AD chip, AD will automatically stop to enter into the waiting state until the next edge of the external clock triggers AD to do the next acquisition, and the conversion is going on in this way, as the diagram following shows:

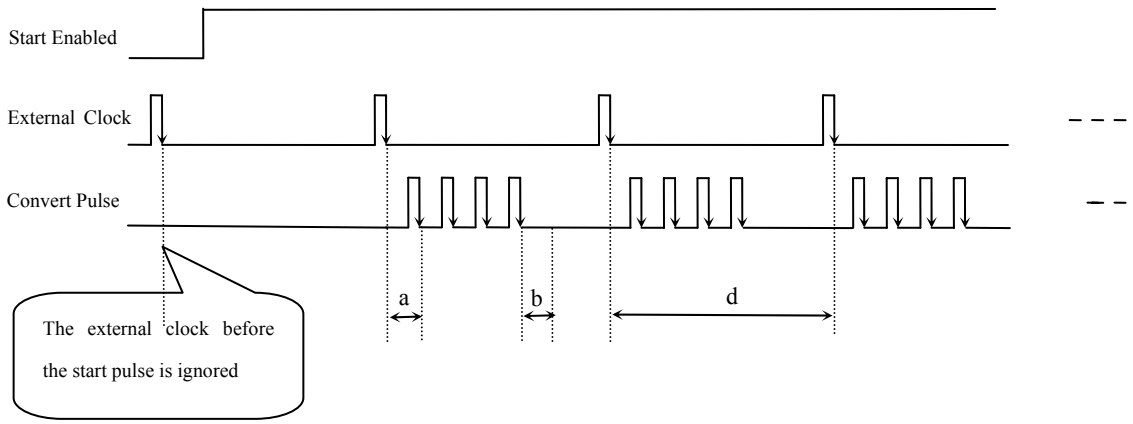


Figure 6.3 Grouping sampling under the fixed frequency external clock mode

Notes: a— internal clock sample cycle
b—AD chips conversion time
d—group cycle（external clock cycle）

Under an unfixed-frequency external clock mode, for example, the grouping sampling principle is the same as that of the fixed-frequency external clock mode. Under this mode, users can control any channel and any number of data.

Users will connect the control signals with the clock input of the card (CLK_IN), set the required sampling frequency and sampling cycles. When there are external clock signals, it will sample the data which is set by users. Because the external clock frequency is not fixed, the size of external clock cycle is inconsistent but to meet: the external clock cycle ≥ the internal clock sampling period × the total number of sampling channels × cycles of group + AD chip conversion time, , otherwise, the external clock edge appearing in the group conversion time will be ignored.

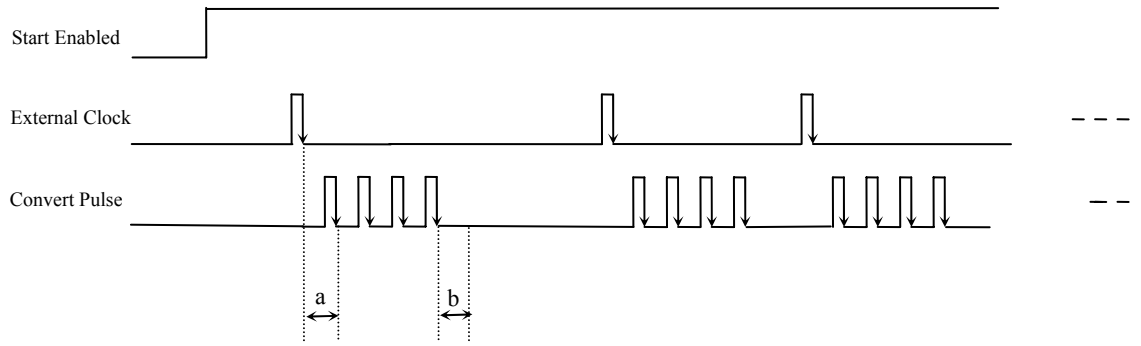


Figure 6.4 Grouping sampling under the not fixed frequency external clock mode

Note: a— internal clock sample cycle
b—AD chips conversion time

Chapter 7 Timer/Counter Function

Mode 0: Interrupt on terminal count

Under this mode, when given the initial value, if GATE is high level, the counter immediately begins to count by subtracting “1” each time, the counter output OUT turns into low level; when the count ends and the count value becomes 0, the counter output OUT becomes and keeps high level until given the initial value or reset. If a counter which is counting is given a new value, the counter will begin to count from the new value by subtracting “1” each time. GATE can be used to control the count, GATE=1 enables counting; GATE=0 disables counting.

OUT signal changes high from low can be used as interrupt request.

Time diagram is shown in Figure 1.

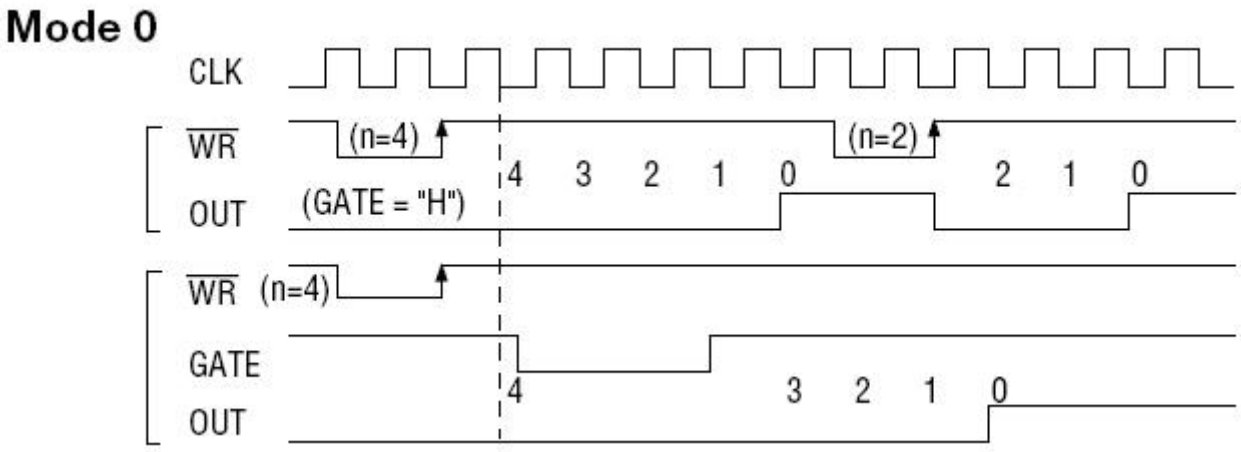


Figure 1

Mode 1: Hardware retriggerable one-shot

The mode can work under the role of GATE. After given the initial count value N, OUT becomes high level, the counter begins to count until the appearance of the rising edge of GATE, at this moment OUT turns into low level; when the count ends and the count value becomes 0, OUT becomes high level, that is, the output one-shot pulse width is determined by the initial count value N. If the current operation does not end and another rising edge of GATE appears, then the current count stops, the counter begins to count from N once again, and then the output one-shot pulse will be widened. When the count reduction of the counter has not yet reached zero, but it is given a new value N1. Only when it is the rising edge of GATE, the counter starts to count from N1.

Time diagram is shown in Figure 2.

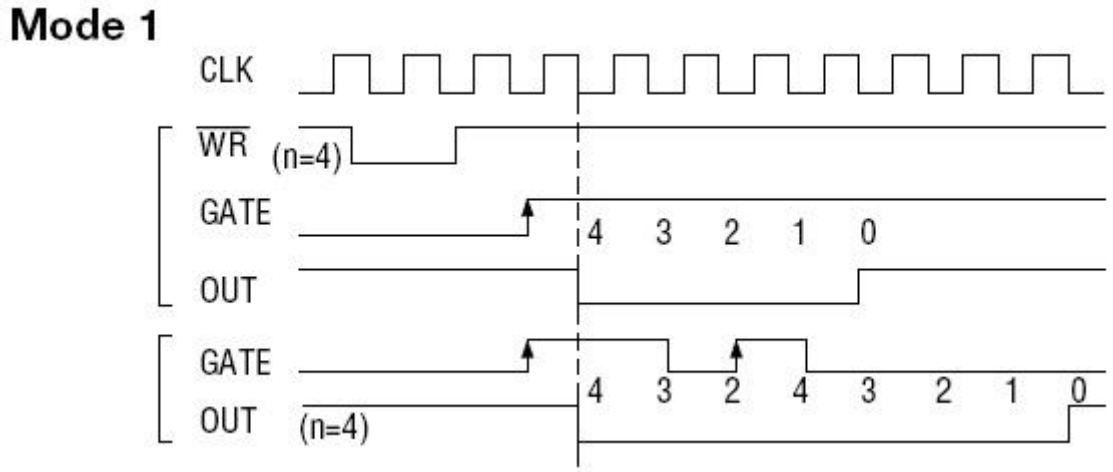


Figure 2

Mode 2: Rate Generator

Under this mode, the counter is given the initial count value N and begins to count from (N-1), OUT becomes high level. When the count value becomes 0, OUT turns into low level. After a CLK cycle, OUT resumes high level, and the counter automatically load the initial value N and begin to count from (N-1). Thus the output will continue to output a negative pulse, its width is equal to one clock cycle, the clock number between the two negative pulses is equal to the initial value that is given to the counter. GATE=1 enables counting; GATE=0 disables counting. GATE has no effect on OUT. If change the initial count when counting, it will be effective next time.

Time diagram is shown in figure 3.

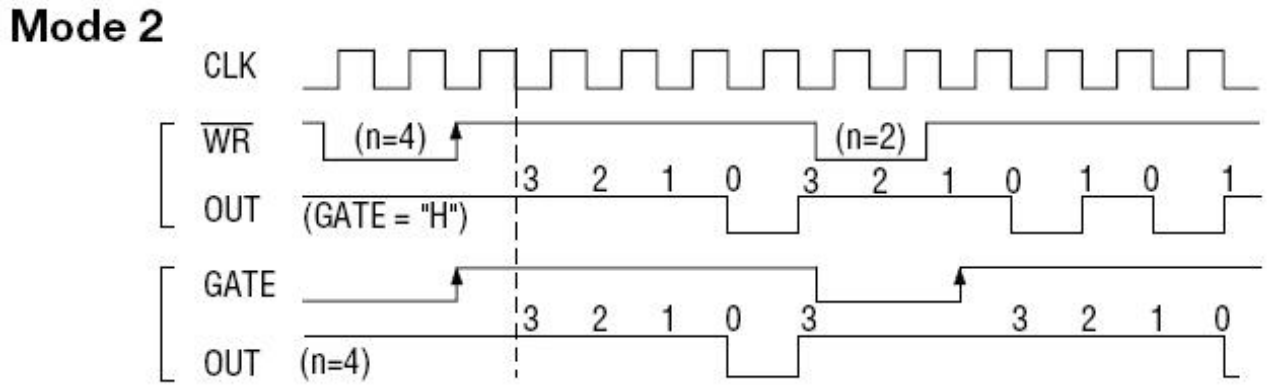


Figure 3

Mode 3: Square wave mode

Similar to Mode 2, the counter is given the initial count value N and begins to count from (N-1). When the signal of GATE is high level, it starts to count, timer/counter begins to count by subtracting “1” each time, more than half the initial count value. The output OUT has remained high level, when the count value is more than half of the initial count value; but the output OUT becomes low level, when the count value is less than half of the initial value. If the initial count value N is an even number, the output is 1:1 square-wave; if the initial count value N is an odd number, the output OUT has remained high level during the previous (n +1)/2 count period; but the output OUT becomes low level during the post (n-1)/2 count period, that is, the high level has one clock cycle more than the low level. If change the initial

count when counting, it will be effective next time. When GATE = 0, the count is prohibited, when GATE = 1, the count is permitted. Time diagram is shown in figure 4.

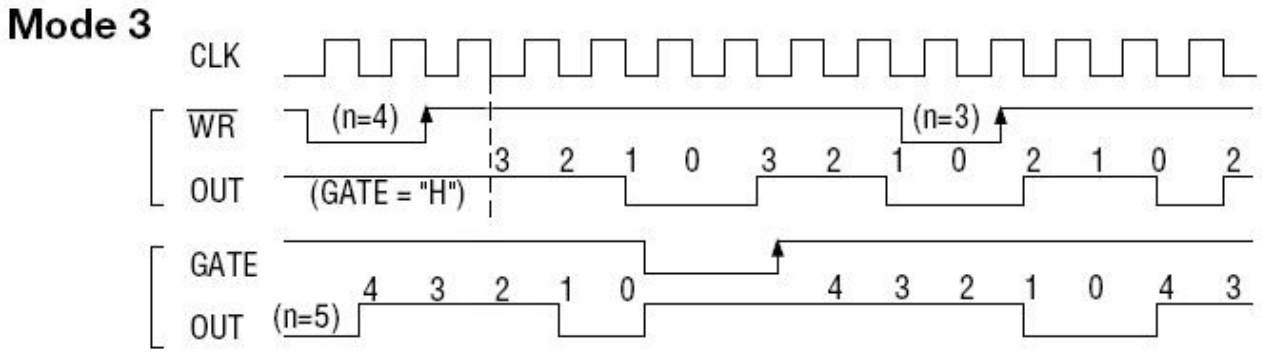


Figure 4

Mode 4: Software triggered strobe

Under this mode, the counter is given the initial count value N and begins to count, the output OUT becomes high level. When the count value becomes 0, it immediately outputs a negative pulse which is equal to the width of one clock cycle. If given a new count value when counting, it will be effective immediately. GATE=1 enables counting; GATE=0 disables counting. GATE has no effect on OUT. Time diagram is shown in figure 5.

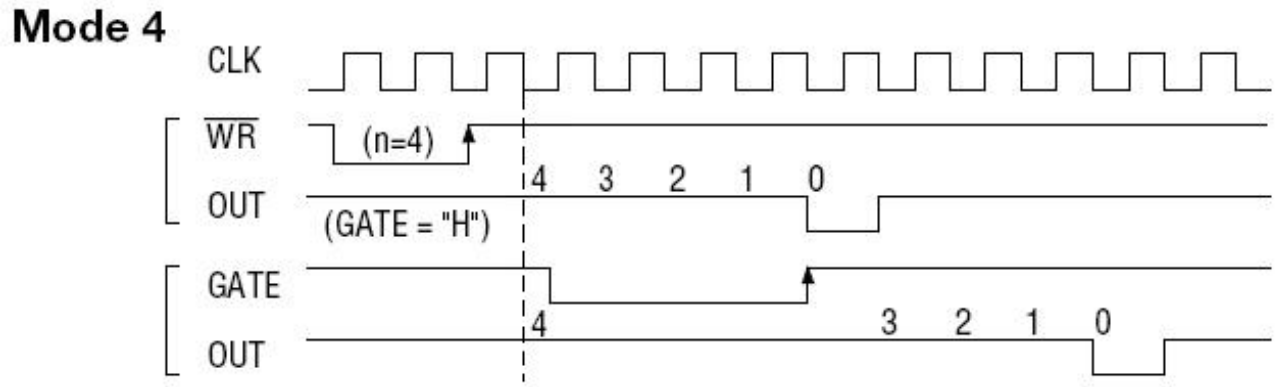


Figure 5

Mode 5: Hardware triggered strobe

Under this mode, when the signal of GATE is on the rising edge, the counter starts to count (so it is called hardware trigger), the output OUT has remained high level. When the count value becomes 0, it outputs a negative pulse which is equal to the width of one clock cycle. And then the rising edge of GATE signal can re-trigger, the counter starts to count from the initial count value again, in the count period, the output has remained high level. When the count reduction of the counter has not yet reached zero, but it is given a new value N1. Only when it is the rising edge of GATE, the counter starts to count from N1. Time diagram is shown in figure 6.

Mode 5

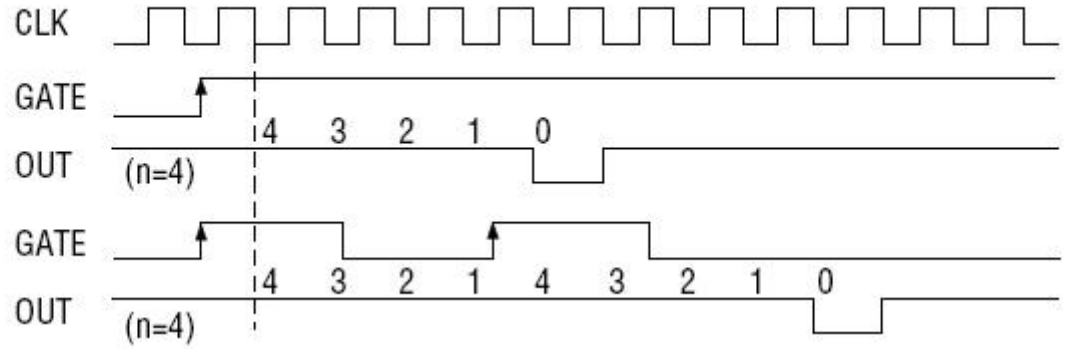


Figure 6

Chapter 8 Address Allocation Table

Address Assignment = base address + offset address

ART2932 register address allocation table

Offset address	Function (Read)	Function (Write)
base address +0x00	D[12:0]:Read AD data from FIFO D[15:13]: Null	First channel[3:0] Last channel[7:4] D[9:8: Gain =00b: 1 time =01b: 2 times =10b: 4 times =11b: 8 times D[15:10]: Reservation
base address +0x02	FIFO status D[0]: EF =1 non-empty =0 empty D[1]:HF =1 not half-full =0 half-full D[2]: FF =1 not overflow =0 overflow	D[0]:Sample Mode =0 Continuous sampling =1 Grouping sampling D[1]: Trigger Mode =0 Software trigger =1 Hardware Trigger D[1]Trigger Source =0 Analog trigger =1 Digital trigger D[3]:Trigger Type =1 Level trigger =0 Edge trigger D[5:4]: Trigger Direction Edge Trigger =00 Falling edge trigger =01 Rising edge trigger =10/11 Either rising or falling edge trigger Level Trigger =00 Low level trigger =01 High level trigger =10/11 Either low or high level trigger D[6]: Clock Source =0 Internal clock =1 External clock D[7]: Clock Output =0 Sample clock output disable =1 Sample clock output enable D[15:8]: Reservation
base address + 0x04	Read back	D [15:0]: set AD sample frequency. Sample rate: 500K (max)

base address +0x06	Read back	D [15:0]: input range control (first write fixed value 0x8020) D[0]: Single-ended and Differential 0: SE 1: DI D[10:1]=0000000000 (fixed value) D[2:0]: Input Range 00: ±10V 01: ±5V 10: ±2.5V 11: 0~10V D[15:13]=101b (fixed value)
base address +0x08	Read back	D[15:0]:Group interval
base address +0x0A	Read back	D[7:0]: Loops of Group D[15:8]: Reservation
base address +0x0C	Read back	D[0]: AD Enable 0: Disable AD 1: Enable AD D[15:1]: Reservation
base address +0x0E	Read back	D[7:0]:Trigger sensitivity D[15:8]: Reservation
base address +0x10	D[15:0]:hardware version (high 16-bit)	Clear FIFO
base address +0x12	D[7:0]:hardware version (low 8-bit)	
base address +0x14	Read Back	Write DA Register [15-0]: DA is 12-bit Power register must be configured to write (write once): 0x001F 1) DA range output register [D15-D3]: Reservation [D2-D0]: Output Range =000: 0~5V =001: 0~10V =010: 0~10.8V =011: ±5V =100: ±10V =101: ±10.8V 2) DA channel selection and data output register [D15-D4]: 12-bit DA data [D3-D0]: Reservation

base address +0x16	Read Back	(Write base address +0X14 first) Write DA register[23-16]: DA is 12-bit Power register must be configured to write (write once): 0x10 we should write the following two registers for each time of DA output. 1) DA output range register [D7-D3]=00001 (fixed value), The range of each channel can be independently controlled. [D2-D0]: DA channel selection = 000: AO0 = 001: AO1 = 010: AO2 = 011: AO3 2) DA channel selection and data output register [D7-D3]=00001 (fixed value) [D2-D0]: DA channel selection = 000: AO0 = 001: AO1 = 010: AO2 = 011: AO3 = 100: All start
base address +0x1A	Read Back	D [15:0]: counter0 initial value
base address +0x1C	D[15:0]: the current value of counter 0	D [2:0]: counter 0 work mode D [15:3]: Reservation
base address +0x1E	Read Back	D [15:0]: counter1 initial value
base address +0x20	D[15:0]: the current value of counter 1	D [2:0]: counter 1 work mode D [15:3]: Reservation
base address +0x22	Read Back	D [15:0]: counter2 initial value
base address +0x24	D[15:0]: the current value of counter 2	D [2:0]: counter 2 work mode D [15:3]: Reservation
base address +0x26	D[7:0]: digital input D[15:8]: null	D[7:0]: digital output D[15:8]: Reservation

Chapter 9 Notes, Calibration and Warranty Policy

9.1 Notes

In our products' packing, user can find a user manual, ART2932 module and a quality guarantee card. Users must keep quality guarantee card carefully, if the products have some problems and need repairing, please send products together with quality guarantee card to ART, we will provide good after-sale service and solve the problem as quickly as we can.

When using ART2932, in order to prevent the IC (chip) from electrostatic harm, please do not touch IC (chip) in the front panel of ART2932module.

9.2 AD Analog Signal Input Calibration

Every device has to be calibrated before sending from the factory. It is necessary to calibrate the module again if users want to after using for a period of time or changing the input range. In the manual, we introduce how to calibrate ART2932 in ±10V, calibrations of other input ranges are similar.

Prepare a digital voltage instrument which the resolution is more than 5.5 bit, install the ART2932 module, and then power on, warm-up for fifteen minutes.

1) Zero adjustment: select one channel of analog inputs, take the channel AI0for example, connect 0V to AI0, and then run ART Data Acquisition Measurement Suite in the WINDOWS. Choose channel 0, ±10V input range and start sampling, adjust potentiometer RP1 in order to make voltage value is 0.000V or about 0.000V. Zero adjustment of other channels is alike.
2) Full-scale adjustment: select one channel of analog inputs, take the channel AI0 for example, connect 9999.69mV to AI0, and then run ART Data Acquisition Measurement Suite in the WINDOWS. Choose channel 0, ±10V input range and start sampling, adjust potentiometer RP2 in order to make voltage value is 9999.69mV or about 9999.69mV. Full-scale adjustment of other channels is alike.
3) Repeat steps above until meet the requirement.

9.3 Analog Signal Output Calibration

In the manual, we introduce how to calibrate ART2932 in ±10V range; calibrations of other ranges are similar.

1) Connect the ground of the digital voltage meter to any analog AGND. Connect the input side of the voltage meter to the output channel which needs calibration. Run ART2932 test procedure under Windows, select the AO output detection.
2) To set DA output 2048, adjust potentiometer RP3 in order to make AO0 output 0.000V.
3) To set DA output 4095, adjust potentiometer RP4 in order to make AO0 output 9995.11mV.
4) Repeat steps above until meet the requirement.

9.4 DA use

In demonstration program, the continuous output interval of waveform output can not be carried out; the main objective is to test the strength of DA output.

9.5 Warranty Policy

Thank you for choosing ART. To understand your rights and enjoy all the after-sales services we offer, please read the following carefully.

1. Before using ART's products please read the user manual and follow the instructions exactly. When sending in damaged products for repair, please attach an RMA application form which can be downloaded from: www.art-control.com.

2. All ART products come with a limited two-year warranty:

- The warranty period starts on the day the product is shipped from ART's factory
- For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. ART is not responsible for any loss of data.
- Please ensure the use of properly licensed software with our systems. ART does not condone the use of pirated software and will not service systems using such software. ART will not be held legally responsible for products shipped with unlicensed software installed by the user.

3. Our repair service is not covered by ART's guarantee in the following situations:

- Damage caused by not following instructions in the User's Manual.
- Damage caused by carelessness on the user's part during product transportation.
- Damage caused by unsuitable storage environments (i.e. high temperatures, high humidity, or volatile chemicals).
- Damage from improper repair by unauthorized ART technicians.
- Products with altered and/or damaged serial numbers are not entitled to our service.

4. Customers are responsible for shipping costs to transport damaged products to our company or sales office.

5. To ensure the speed and quality of product repair, please download an RMA application form from our company website.

Products Rapid Installation and Self-check

Rapid Installation

Product-driven procedure is the operating system adaptive installation mode. After inserting the disc, you can select the appropriate board type on the pop-up interface, click the button【driver installation】; or select CD-ROM drive in Resource Explorer, locate the product catalog and enter into the APP folder, and implement Setup.exe file. After the installation, pop-up CD-ROM, shut off your computer, insert the PCI card. If it is a USB product, it can be directly inserted into the device. When the system prompts that it finds a new hardware, you do not specify a drive path, the operating system can automatically look up it from the system directory, and then you can complete the installation.

Self-check

At this moment, there should be installation information of the installed device in the Device Manager (when the device does not work, you can check this item.). Open "Start -> Programs -> ART Demonstration Monitoring and Control System -> Corresponding Board -> Advanced Testing Presentation System", the program is a standard testing procedure. Based on the specification of Pin definition, connect the signal acquisition data and test whether AD is normal or not. Connect the input pins to the corresponding output pins and use the testing procedure to test whether the switch is normal or not.

Delete Wrong Installation

When you select the wrong drive, or viruses lead to driver error, you can carry out the following operations: In Resource Explorer, open CD-ROM drive, run Others-> SUPPORT-> PCI.bat procedures, and delete the hardware information that relevant to our boards, and then carry out the process of section I all over again, we can complete the new installation.